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# HARD IP CORE OF MEMORY ARBITER

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**Abstract**: This paper deals with the design of 4X4 memory arbiter and its results. The memory arbiter is completely optimized from synthesis till VLSI layout design. The designed block of 4X4 arbiter can be re used as a component to have N number of clients. Memory arbiter is an important system for controlling multiple requests. It works according to the priority of the request.

**Keywords**: arbiter, priority encoder, round robin, vlsi technology

## I. INTRODUCTION

To cope up with the present market needs and time to market IP core development helps a lot in increasing the efficiency and speed of product development. Any decision making device is termed as arbiter. Hard IP Core deals with with entire cycle of product design and layout design of that particular product. Arbiter is of prime importance in the following fields,

I. At the time of shared memory usage
II. In network switching where multiple input ports use a common bus
III. When multiple processors working on different clocks are to be synchronized.

Round Robin Architecture is implemented in this design to provides cyclic priorities to all the users of the system.

## II. ROUND ROBIN ARCHITECTURE

In this type of arbiter priority is cyclic in nature. It keeps on changing at every clock cycle. It is more efficient and widely used system than fixed priority. Here no client is considered the most important and so each client gets equal chance for getting their request completed.

Since it is cyclic in nature it is also named as Cyclic Arbitration.

Advantages of Round Robin Arbiter are

- Maximum delay in granting client's request is C-1 where C is the number of clients/requests.
- Starving of clients does not take place.
- No user biasing is prevalent.

Disadvantages of Round Robin Arbiter are

- Request of prime importance can be missed to due to cyclic priority.
- Complexity of the design is higher than fixed priority.

## III. WORKING OF 4X4 ARBITER

As shown in Fig 1 memory arbiter consists of seven inputs and 4 outputs with any one active output at a time.

In the development of memory arbiter round robin arbiter design is implemented. 4-bit vector 'a' represents four client requests, 'eot' represents the completion of memory usage by a particular client, 4-bit vector 'o' represents the grant provided to the client (i.e. g(0) for a(0), g(1) for a(1) and so on). For synchronous working a common clock is provided. Now depending on the priority of the client the access to the memory to each client is provided. In round robin method, the priority of the clients keeps on changing so that each client gets the benefit of quick memory access. For a fixed time slot one client is provided with highest priority while for the second slot another client is provided with highest priority. To achieve this rotating priority structure a ring counter is implemented with mealy state machine and accordingly each time one of the priority logic blocks is implemented in each time slot. The time slot provided keeps on varying depending upon the time till which the current client is accessing the memory. When the client provides an 'eot' signal new client is taken care of. Maximum waiting time for any client is M-1 time slots where M is number of clients (here M=4 so total 3 time slots).

A VHDL code was written on Xilinx 10.2 along with the test bench to simulate the result. The working of the arbiter was checked on FPGA kit and found to be working properly. Also its RTL view was simulated for the layout design.

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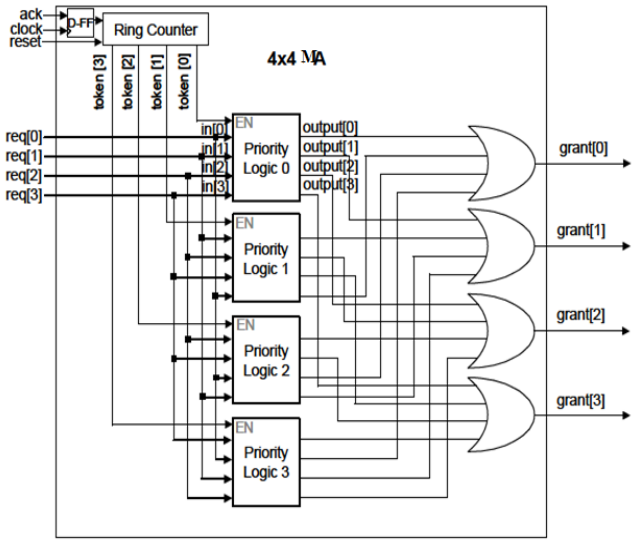


Fig. 1 Block Diagram of Memory Arbiter

## IV. CONCLUSION

Microwind layout design tool was used to implement the Gate Level Schematic using 0.12 micron technology. Following design results were obtained –

- 16 Multiplexers
- 16 positive edge triggered D-Flip flops before every MUX to latch input
- One FSM (Finite State Machine) made up of 4 edge triggered D-Flip flops to change states.
- Four, 4 input OR gate to combine results of 4 MUX each. The output of each OR gate is latched by one edge triggered D-Flip flop.
- The total gate count of MUX is **48**. Out of which **32** are multiple input AND gates and **16** are two input OR gates.
- Overall gate count is 217.
- Area utilized was 1090λ (65.400µm) * 1030λ (61.800µm) = 1122700 $\lambda^2$ (4041.72µm$^2$).
- 1 λ = 0.06 µm.
- Power dissipation was found to be 3.671 mW.
- Voltage levels are 1.20V for input high and 0V for input low.
- Technology used is CMOS 0.12µm.
- Clock frequency is 0.5128GHz.
- The triggering pulse for FSM is having width of 0.475 ns. Its start time is 0.475ns.
- All input signals are having rise-time and fall time of 0.025ns.
- W/L of each nMOS is1.

Fig. 2 shows the simulation result

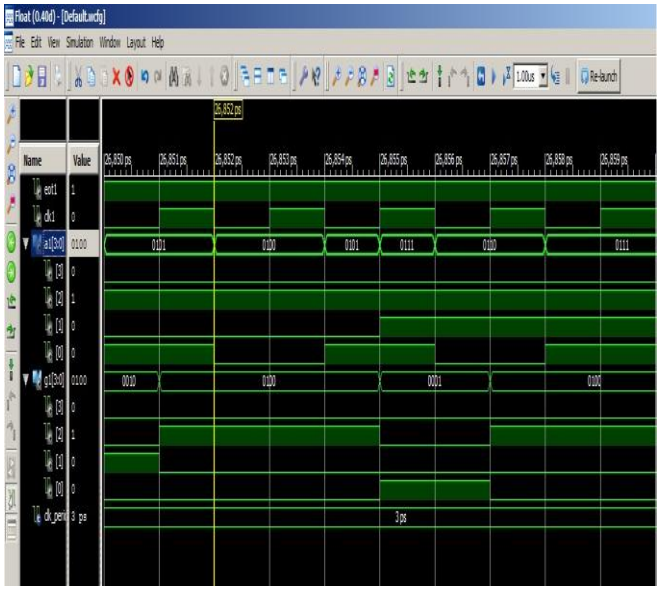

Fig. 2 Simulation Result

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We thank God for filling us with positivity. We thank our Sad Guru Bhagwan Pujya Morari Bapu and our parents for bestowing us with their blessings.

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